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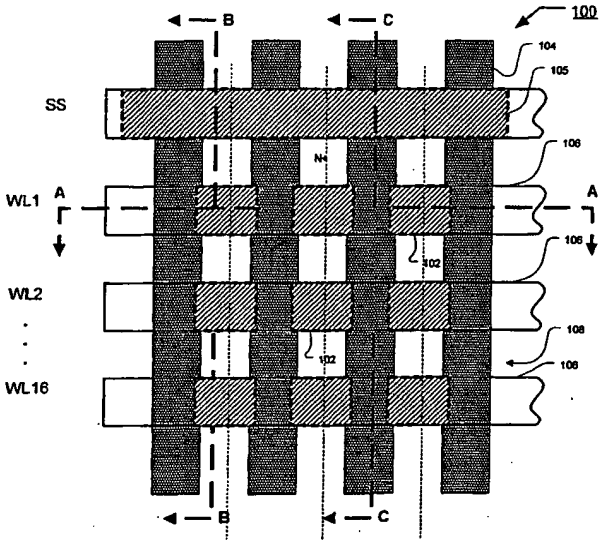
(54) Title: DEEP WORDLINE TRENCH TO SHIELD CROSS COUPLING BETWEEN ADJACENT CELLS FOR SCALED NAND



(57) Abstract: A NAND flash memory structure with a wordline or control gate that provides shielding from Yupin effect errors and generally from potentials in adjacent strings of transistors undergoing programming operations with significant variations in potential. Each string has a first select gate (105), a plurality of floating gates (102), and a second select gate. The floating gates are formed between shallow trench isolation areas (104) and wordlines (106) extend across adjacent strings and extend between the floating gates into the shallow trench isolation areas thereby shielding the floating gates from variations in potential of adjacent memory cells.

WO 2004/001852 A1

DEEP WORDLINE TRENCH TO SHIELD CROSS COUPLING BETWEEN ADJACENT CELLS FOR SCALED NAND

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates generally to flash electrically erasable and programmable read only memory (EEPROMS), and more specifically to NAND flash memory with a high memory cell density.

Related Art

[0002] Most existing commercial flash EEPROM products operate each memory cell with two ranges of threshold voltages, one above and the other below a breakpoint level, thereby defining two programmed states. One bit of data is thus stored in each cell, a 0 when programmed into one state and a 1 when programmed into its other state. A chunk of a given number of bits of data is programmed at one time into an equal number of cells. The state of each cell is monitored during programming so that application of programming voltages stops when the threshold level of an individual cell is verified to have moved within the range that represents the value of the bit of data being stored in the cell.

[0003] In order to increase the amount of data stored in a flash EEPROM system having a certain number of storage cells, the individual cells are operated with more than two threshold level states. Preferably, two or more bits of data are stored in each cell by operating the individual cells with four or more programmable states. Three threshold breakpoint levels are necessary to define four different threshold states. Such a system is described in U.S. Patent Nos. 5,043,940 and 5,172,338, which are hereby incorporated by this reference in their entirety. In multi-state operation, an available operating voltage range of the individual cells is divided into an increased number of states. The use of eight or more states, resulting in storing three or more bits of data per cell, is contemplated. The voltage range of each state necessarily becomes smaller as the

number of states is increased. This leaves less margin within each state to accommodate any error that might occur during operation of the memory system.

[0004] One type of error is termed a "disturb," wherein electrons are unintentionally added to or taken away from a floating gate during operation of the memory. One source of a disturb is the presence of a leaky oxide dielectric positioned between the floating gate and another conductive gate of a cell. The charge level programmed onto a floating gate of a cell changes when such a leaky oxide is present, thus leading to the possibility that the state of the cell will be incorrectly read if the change in charge has been large enough. Since few to no errors can be tolerated in a mass digital data storage system, a sufficient margin for this error is provided by making the voltage range allocated to each state sufficient to include an expanded range of voltages that can occur as the result of such disturbs. This necessarily limits the number of states that can be included in a multi-state flash EEPROM system since the total available voltage range is limited.

[0005] Another type of error is termed the "Yupin effect." The Yupin effect occurs when the neighboring cell of a selected cell is programmed after the selected cell itself is programmed, and the charges of the neighboring cell influence the voltage of the selected cell. Any potential present in an adjacent cell or string may influence the reading of a selected cell, including those in the channel, floating gate, or control gates etc... Such interference from the subsequently programmed neighbor cell distorts the voltages of the selected cell, possibly leading to an erroneous identification of its memory state during reading.

SUMMARY OF THE INVENTION

[0006] The present invention is an improved structure for high density NAND type flash memory that minimizes the effect of disturbs and Yupin effect errors.

[0007] One aspect of the invention is a NAND flash memory device formed from a substrate. The device comprises strings of transistors. Each string has a first select gate, a plurality of floating gates, and a second select gate. The floating gates are formed between shallow trench isolation areas and wordlines extend across adjacent strings and extend between the floating gates into the shallow trench isolation areas thereby isolating adjacent floating gates. The wordlines shield a selected floating gate from the potentials, and from variations in the potentials of adjacent memory cells and components. The

electric fields may emanate from a component located anywhere near the selected floating gate, for example above or below or at a diagonal.

[0008] Another aspect of the invention is a flash memory device formed from a substrate. The device comprises strings of adjacent transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate, the plurality of floating gates formed above the substrate, wherein the strings are separated by shallow trench isolation areas. The device has two or more discrete programming levels programmed by increasing a programming potential until the levels are reached, wherein once the floating gates have reached a steady state a linear increase in programming potential results in an approximately linear increase in floating gate charge given a constant potential surrounding environment. Wordlines extend across adjacent strings and between the floating gates into the shallow trench isolation areas, such that when a floating gate of a selected string is read or verified, the wordline minimizes deviation from the linear increase due to voltage variations in the surrounding environment.

[0009] The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings of illustrative embodiments of the invention.

BRIEF DESCRIPTION OF THE FIGURES

[0010] FIG. 1A is a plan view of the structure of memory array 100.

[0011] FIG. 1B is an electrical circuit diagram corresponding to the structure of FIG. 1A.

[0012] FIG. 2 is a cross section of memory array 100.

[0013] FIG. 3 is a cross section of memory array 100.

[0014] FIG. 4 is a cross section of memory array 100.

[0015] FIG. 5A is a plot of program voltage vs. time during a program operation.

[0016] FIG. 5B is a plot of the voltage distribution of programming steps.

[0017] FIG. 5C is a plot of cell voltage vs. program voltage.

[0018] FIG. 5D is an illustration of an adjacent memory cell during a program operation.

[0019] FIG. 5E is an illustration of an adjacent memory cell during lockout.

[0020] FIG. 6 is a flow chart of a method of forming an embodiment of the present invention.

[0021] FIGS. 7A-7L are cross sections of memory array 100 at various stages during the fabrication process.

DETAILED DESCRIPTION OF THE INVENTION

[0022] The following is a detailed description of illustrative embodiments of the present invention. As these embodiments of the present invention are described with reference to the aforementioned drawings, various modifications or adaptations of the methods and or specific structures described may become apparent to those skilled in the art. All such modifications, adaptations, or variations that rely upon the teachings of the present invention, and through which these teachings have advanced the art, are considered to be within the scope of the present invention. Hence, these descriptions and drawings are not to be considered in a limiting sense, as it is understood that the present invention is in no way limited to the embodiments illustrated.

[0023] FIG. 1A illustrates a plan view of an embodiment of the NAND flash memory of the present invention. FIGS. 2-4 are cross sections taken through the structure shown in FIG. 1A. An electrical equivalent circuit of the memory array is given in FIG. 1B, wherein common elements within the structure of FIGS. 1A and 2-4 are identified by the same reference character.

[0024] Parallel wordlines 106 connect adjacent NAND strings of floating gates 102. The wordlines 106 are illustrated horizontally, and the strings are illustrated vertically in the figures. A NAND string generally includes a select gate followed by several floating gates and another select gate. The bitline A, B, and C (BL_A, BL_B, BL_C) locations correspond to the string locations in the plan view, although the bitlines are generally located in another plane. The circuit diagram of FIG. 1B most clearly shows the vertical array of strings. In this case sixteen floating gates and thus sixteen wordlines are illustrated per string, however, the number of floating gates may be thirty-two or more, and is foreseen to increase in the future. Floating gates 102 are isolated from adjacent floating gates by isolation trenches 104. Isolating trenches 104 are also referred to as

shallow trench isolation areas. The select gate line 105 on the source side ("SS") is continuous between trenches 104, as can be seen in section C-C of FIG. 4. It is not etched into individual floating gates. At the end of the wordline 106 above SS 105, each NAND string is electrically connected to SS 105 with a via, most easily seen in FIG. 1B an FIG. 3.

[0025] Metal bitlines 116 (only one of which is shown for the sake of clarity) connect to the N+ regions 114 within substrate 108 to sense amplifiers for reading the charge stored in the floating gates 102. Thus, to read a particular floating gate a string is selected via the bitline and a wordline is also selected. The metal bitlines are generally, but not necessarily, formed in a conductive layer insulated from the wordlines. At the end of each string is another select gate coupled to the drain ("SD"). The drain and source can be interchanged in some configurations and more than 16 transistors can also be present in each string, thus also increasing the number of wordlines.

[0026] As seen in FIG. 2, there is a portion of gate oxide 112 between each floating gate 102 and the substrate 108. A dielectric material 110 separates the wordlines 106 from the floating gates 102 and the isolation trenches 104. Adjacent floating gates 102 are isolated from other floating gates in the same wordline, not only by isolating trenches 104, but also by wordlines 106. Wordlines 106 extend down between floating gates into isolation trenches 104, until, within, or past the level of gate oxide layer 112. This has several distinct benefits.

[0027] It reduces Yupin effects between adjacent cells in the wordline direction. Also, it improves the cell coupling ratio between the wordlines and the floating gates. The portion of the wordline that extends into the isolation trenches, to or past the depth of the floating gates, increases the overlap of the surface areas and volumes of the wordlines and floating gates. This increased overlap results in better coupling when a charge is read or stored during program, read, or erase operations.

[0028] The electrical field across the dielectric layer 110 between adjacent floating gates is reduced, therefore reducing any leakage current through the dielectric layer that may occur as a result of the electrical field. The lesser the electrical field, the lesser the leakage current between two adjacent floating gates. Additionally, the leakage current path is greatly increased by the extended wordlines 106. Any leakage current must travel

down and around the extended portion of the wordlines and then back up or over to the adjacent floating gates. The charge level programmed onto a floating gate of a cell changes when such a leakage current is present. Therefore, by minimizing the leakage current, and thus any change in charge of the floating gates, an increased number of levels can be discerned more reliably. This leads to a higher capacity, more cost efficient, and more reliable data storage system.

[0029] Additionally, the extended wordline shields a selected floating gate from field effects of nearby channels. In certain program, read, and verify operations, a floating gate that has been programmed with a particular charge may, in a subsequent read or verify operation, indicate that it has a larger charge than it should due to a potential or charge in an adjacent channel. This is especially true with complicated program, read, and verify operations in multi-state NAND flash memory where multiple operations are occurring simultaneously in adjacent strings and cells.

In many prior systems, every other cell along one row is part of the same page; in newer systems, every cell along one row can be part of the same page. Referring again to FIG. 2, this would mean that in a prior system, the floating gate 102A activated by BL_A and the floating gate 102C activated by BL_C would be programmed while the floating gate 102B activated by BL_B is not programmed. In newer systems, every cell along one row can be part of the same page. Thus, as seen in FIG. 2, floating gate 102A of the string activated by BL_A may be undergoing a programming operation at the same time as floating gate 102B. This will be discussed in further detail later in reference to FIGS. 5D and 5E. In this way, twice the number of cells may be programmed and or verified at the same time. Although this may be efficient, it results in additional field effect problems during all of the various operations involved in data storage operations.

[0030] The relationship between the distribution and the incremental voltage of the programming pulses holds true only if the potential of any other coupling element to the floating gates of the cells being programmed remains constant. In the case of programming adjacent NAND strings, an adjacent (substrate) channel of an adjacent cell may be at a low potential, for instance 0V, for a number of programming pulses while it is being programmed and then suddenly be boosted or "locked out" for subsequent programming pulses to a high potential, for instance, 5, 7.5, or 10 V, after it verifies in order to stop further programming or for any other reason. This boosting of the channel

potential also increases the floating gate potential of the adjacent cell. Thus, both the adjacent channel and adjacent floating gate will couple a higher potential to the selected cell for the next programming pulse which may broaden the width of the programmed distribution. This has a number of negative consequences, some of which may include error in reading a particular bit and reduction in the total number of bits of data that may be stored in a given die size. An example of some programming details is illustrated in FIGS. 5A-5E which will be discussed below. The levels given are illustrative and only serve to educate the reader on the operation of an example memory system with which the present invention may be particularly advantageous.

[0031] For further information regarding the data storage operations, please refer to . U.S. Patent Application Serial No. 09/893,277, filed June 27, 2001, entitled "Operating Techniques For Reducing Effects Of Coupling Between Storage Elements Of A Non-Volatile Memory Operated In Multiple Data States," hereby incorporated by this reference in its entirety, and an article entitled "Fast and Accurate Programming Method for Multi-level NAND EEPROMs", pp. 129-130, *Digest of 1995 Symposium of VLSI Technology*, which is also hereby incorporated by this reference in its entirety, and discusses the timing and voltage levels of programming pulses using in the read/verify and programming operations.

[0032] An example of the incremental voltage steps of the programming pulses are shown in FIG. 5A. In the example shown and described, the pulses are incremented by 0.2 volts. After each pulse, there is a verify cycle, followed by an incrementally higher voltage pulse. This takes place until a desired or threshold voltage is verified in the floating gate. For example, this may take place until the floating gate is verified at 2.0 volts.

[0033] FIG. 5B illustrates that for each program pulse, there is a distribution of the charge stored in the floating gates. For example, with the first pulse of 16.0 volts, the distribution of the verified charges is about three volts. So, if it is desired to store 2.0 volts on the floating gate, it may be necessary to increment up to 17.0 volts and higher in the control gate or wordline. If, for example, after a 17.0 volt programming pulse the distribution of stored charges on the floating gates is such that there are some floating gates above and some below the 2.0 V threshold, those below will receive a further programming while those above the threshold will not by having their channel boosted or

"locked out."

[0034] With a constant environment, i.e. one where the potential and electric field of the neighboring components is constant, the programming pulses, will, after having reached a steady state, result in a predictable and approximately linear increase in the cell voltage (V_t), as seen in FIG. 5C. As seen in the nearly parallel lines, some "fast" floating gates may reach the desired verify V_t at a lower program voltage than other "slow" or "intermediate" floating gates. Once the steady state has been reached, it can be seen that a linear increase in the program voltage results in a nearly linear increase in V_t.

[0035] Therefore, if, for example, a cell has a V_t of 1.99 volts, it will receive another programming pulse to take it above the 2.0 volt threshold. In a constant environment, the cell should then have a V_t of 2.19 volts. However, if there is any deviation of the voltage or electric field that is applied to the cell, for example between one programming pulse and another, the voltage stored on the cell may differ from that expected. If a neighboring component exerts an influence of the electrical field of the cell during a programming pulse, the charge stored will also deviate. For example, the cell that was at 1.99 volts in the previous verification cycle, may instead of having a V_t of 2.19 volts may have a V_t of 2.29 or 2.39 volts. As shown in FIG. 5C, coupling of potential from a nearby cell may cause one of the intermediate cells to deviate from the linear increase that is characteristic of the steady state. Thus, the distribution of the cells shown in FIG. 5B will increase due to any variation in the potential of adjacent components.

[0036] The increase in the distribution of cells will lessen the number of states that can be repeatably and reliably discerned in a multi-level storage system. This greatly lessens the storage capacity of a memory device with a given die size, and therefore increases the cost of production of a storage device with a desired storage capacity.

[0037] Specifically, as can be seen in FIGS. 5D and 5E, the voltages in the components of an adjacent cell will vary greatly during program and during "lockout." An adjacent cell is any cell located near another cell, in any direction, including diagonally. For example, floating gate 102A is adjacent to floating gate 102B. The active area of the cell comprises the channel area in the substrate below the floating gate and the wordline area above the floating gate. The cell may also be said to comprise portions of the shallow trench isolation area and other components. A cell is "locked out" by isolating its

corresponding bitline if it has verified at the desired program voltage. In the example given above, if the cell has verified at 2.0 volts, it will be "locked out" from further programming pulses by increasing the cell voltage in the channel (substrate) to a relatively high voltage level by isolating the corresponding bitline.

[0038] FIG. 5D shows an adjacent cell during the programming operations previously discussed. The shape and configuration of the cells is simplified for ease of understanding. In the example programming operation shown, wordline 106 of the cell is at 18 volts, floating gate 102 is at 10 volts, and substrate 108 is at 0 volts. However, during lockout, as shown in FIG. 5E, wordline 106 is now at 18.2 volts, floating gate 102 is now at 13 volts, and substrate 108 is now at 8.0 volts. The channel is a portion of the substrate just below the upper surface of the substrate. While a selected cell is being programmed, an adjacent cell may be either in the program operation shown in FIG. 5D, or the lockout state shown in FIG. 5E. Furthermore, the voltages shown in the program operations vary with the different programming pulses discussed earlier. All of these voltages shown in an adjacent cell may couple to a selected cell during programming. It is the variation in these voltages that may result in the variation from steady state programming (FIG. 5C) and thus increased deviation (FIG. 5B).

[0039] FIG. 6 is a flowchart of the steps of making memory array 100 which should be referred to in tandem with FIGS. 7A-7L. The memory array 100 is fabricated in a substrate 108. Substrate 108 preferably comprises silicon but may also comprise any material known to those in the art such as Gallium Arsenide etc... First, a gate oxide layer 112 is formed upon substrate 108 in step 505 as seen in FIG. 7A. Gate oxide 112 is preferably grown on substrate 108 but may also be deposited. Gate oxide layer 112 preferably comprises silicon dioxide but may differ depending on what type of substrate is used and other processing factors or elements introduced during processing. For example, for CMOS applications, gate oxide 112 may comprise materials (known as ETO) including nitride/oxynitride. Next, a first gate layer 102a is deposited upon gate oxide layer 112 in step 510 as seen in FIG. 7B. The first gate layer 102a is made of semiconducting material such as polysilicon. A nitride layer 120 is then deposited upon the first floating gate layer 102a in step 515 as seen in FIG 7C. In step 520, parallel trenches are etched in substrate 108 with well known etching techniques. Generally in fabricating high density memory arrays where the features are of a very small scale, plasma etching is preferred over wet etching in order to have a precise and uniform etch.

In step 525 the trenches are then filled with a field oxide, as seen in FIG. 7D, to form isolation trenches 104. The field oxide within isolation trenches 104 is preferably comprised of silicon dioxide but can be comprised of other insulating materials (including materials other than oxides). Isolation trenches 104 range from about 0.2 microns to about 0.25 microns wide and are preferably about 0.2 microns wide. The remaining field oxide 124 is removed via chemical-mechanical polishing ("CMP") in step 530, as seen in FIG. 7F.

[0040] Next, in step 535, nitride layer 120 is etched away such that isolation trenches 104 extend above the surface of the first gate layer 102a, as seen in FIG 6G. The isolating trenches 104 may extend above the substrate 108 and gate oxide layer 112 as shown, or, alternatively, may only extend up to the level of either the substrate 108, gate oxide layer 112, or first gate layer 102a, and it should be understood that differing processes and steps may be necessary to achieve these differing embodiments.

[0041] A second gate layer 102b of the same semiconducting material as the first gate layer 102a is then deposited upon the gate oxide layer 112 and isolation trenches 104 in step 540. It is then selectively etched above isolation trenches 104 to create floating gates 102 in step 545. The resultant structure can be seen in FIG. 7H. Floating gates 102 are substantially "T" shaped in order to maximize the coupling between the floating gate and the control gate, also referred to as the wordline 106 that activates the floating gate. The line between the first and second gate layers 102a and 102b has been removed for the sake of clarity. The T shape provides a large surface area between floating gate and the wordline, thus maximizing the coupling ratio between the two devices for improved read, program and erase operations. For further information, please refer to co-pending U.S. Patent Application No. 09/925,102 to Yuan et al., entitled "Scalable Self-Aligned Dual Floating Gate Memory Cell Array and Methods of Forming the Array," which is hereby incorporated by this reference in its entirety.

[0042] As seen in FIG. 7J, a set of parallel trenches 122 is formed within isolating trenches 104 in step 550. Trenches 122 may extend within trenches 104 to the level of the upper surface of gate oxide 112 or any distance within trenches 104 within or below the level of gate oxide 112. Isolation layer 110 is then deposited upon the floating gates 102, and within second trenches 122 in isolation trenches 104, in step 555, as seen in FIG 7K. Isolation layer 110 is preferably a dielectric layer such as an oxide-nitride-oxide

("ONO") layer 110. The dielectric layer 110 can be any type of dielectric known in the art and is not necessarily limited to an ONO structure. A wordline layer comprising a semiconducting material layer such as polysilicon and a conductive layer such as tungsten silicide is then deposited upon dielectric layer 110 in step 560, as can be seen in FIG. 7L. Wordlines 106 are then etched from the wordline layer in step 565.

[0043] As previously mentioned, the wordlines 106 extend down between the floating gates 102 into the isolating trenches 104. This isolates adjacent floating gates 102 from each other. In the preferred embodiment, wordlines 106 extend within the isolation trenches 104 to or beyond the level of the gate dielectric 112.

[0044] The various layers can be formed and the etching steps can be performed in many different well known methods and orders, and are not necessarily done in the order described, i.e. gate oxide layer 112 may be formed before or after the parallel trenches are etched into substrate 108 etc... Furthermore, additional layers, steps, and resultant structures that are not described may also be part of the process and the resultant memory array.

[0045] The extended wordline reduces the problem of the aforementioned Yupin effect because it acts as a shield between adjacent floating gates. Again, in short, the Yupin effect is when the charge stored or otherwise present in a neighboring cell influences the reading of a selected cell. The present solution shields gates to avoid or minimize Yupin effect errors caused by neighboring gates. Yupin effect errors can also be accommodated through program and read circuitry and algorithms.

[0046] The extended wordline also protects against conduction leakage between adjacent floating gates within the dielectric layer 110 because it blocks the conduction path between adjacent gates. Furthermore, any possible stringers as a result of an incomplete etch of the floating gate layer that might short circuit adjacent gates are also eliminated in the situation where the etch within the isolation trench extends past the upper (top of the "T") portion of the T shaped floating gate. For more information on the Yupin effect and on disturbs, please refer to U.S. Patent No. 5, 867,429, which was previously incorporated by reference.

[0047] While embodiments of the present invention have been shown and described, changes and modifications to these illustrative embodiments can be made without

departing from the present invention in its broader aspects. Thus, it should be evident that there are other embodiments of this invention which, while not expressly described above, are within the scope of the present invention and therefore that the scope of the invention is not limited merely to the illustrative embodiments presented. Therefore, it will be understood that the appended claims set out the metes and bounds of the invention. However, as words are an imperfect way of describing the scope of the invention, it should also be understood that equivalent structures and methods while not within the express words of the claims are also within the true scope of the invention.

CLAIMS

A flash memory device formed from a substrate, the device comprising:

strings of adjacent transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate, the plurality of floating gates formed above channel regions in the substrate and separated from the channel regions,

wherein adjacent first and second strings undergo programming operations at the same time, and wherein when programming a selected cell of the first string, any change in the potential in the second adjacent string is shielded from the first string by wordlines extending across adjacent strings and extending between the floating gates of the first and second strings into the shallow trench isolation areas between the channel regions of adjacent strings to shield a floating gate of a first string from a potential of a second adjacent string.

2. The flash memory device of claim 1 wherein the wordline shields the floating gate of the first string from a potential in the substrate at an adjacent second string.

3. The flash memory device of claim 1 wherein the wordline shields the floating gate of the first string from a potential of the adjacent floating gate of the second string.

4. The flash memory device of claim 1 further comprising a gate oxide layer between the floating gates and the substrate, the wordline extending down past the level of an upper surface of the gate oxide layer.

5. The flash memory device of claim 1 wherein the wordline shields the floating gate of the first string from the potential of a floating gate of the second adjacent string.

6. A flash memory device comprising:

strings of adjacent transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate, the plurality of floating gates formed above a substrate;

shallow trench isolation areas between the strings;

wordlines extending across adjacent strings and extending between the floating gates into the shallow trench isolation areas between the strings,

wherein in the case of programming adjacent NAND strings, a channel of a first string adjacent a floating gate of a second string may be at a first potential for a number of programming pulses and changed to a second potential during subsequent programming pulses, and

wherein the potential of the channel of the first string may couple to the potential of the floating gate of the second string, and

wherein the wordline shields the floating gate of the second string from the potential of the channel of the first string.

7. The flash memory device of claim 6 further comprising a gate oxide layer between the floating gates and the substrate, the wordlines extending down past the level of an upper surface of the gate oxide layer.

8. The flash memory device of claim 6 wherein the wordlines extend down past the level of an upper surface of the substrate.

9. The flash memory device of claim 6 wherein the wordlines extend down past the lower level of the channel.

10. A flash memory device formed from a substrate, the device comprising:

strings of adjacent transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate, the plurality of floating gates formed above the substrate,

the floating gates formed above a gate oxide layer formed upon cell channel regions within the substrate;

control gates that extend across adjacent strings and between the floating gates of adjacent strings, each control gate extending down past an upper surface of the substrate

to shield a selected floating gate during a read or verify operation from the potential present in an adjacent string.

11. The flash memory device of claim 10 wherein the control gates shield the selected floating gate from the potential of the substrate beneath the adjacent string.

12. The flash memory device of claim 11 wherein the control gates shield the selected floating gate from the potential of a channel region of the substrate beneath the adjacent string.

13. The flash memory device of claim 10 wherein the control gates shield the selected floating gate from the potential of the floating gates of the adjacent string.

14. A flash memory device formed from a substrate, the device comprising:

strings of adjacent transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate, the plurality of floating gates formed above the substrate, wherein the strings are separated by shallow trench isolation areas;

two or more discrete programming levels programmed by increasing a programming potential until the levels are reached, wherein once the floating gates have reached a steady state a linear increase in programming potential results in an approximately linear increase in floating gate charge given a constant potential surrounding environment; and

wordlines extending across adjacent strings and extending between the floating gates into the shallow trench isolation areas,

such that when a floating gate of a selected string is read or verified, the wordline minimizes deviation from the linear increase due to voltage variations in the surrounding environment.

15. The flash memory device of claim 14 wherein the wordline shields the floating gate of the selected string from voltage variations in an adjacent portion of the substrate.

16. The flash memory device of claim 14 wherein the wordline shields the floating gate of the selected string from voltage variations in an adjacent floating gate.

17. The flash memory device of claim 14 wherein the wordline shields the floating gate of the first string from the potential of the channel region of the second adjacent string.

18. The flash memory device of claim 14 further comprising a gate oxide layer between the floating gates and the substrate, the wordline extending down past the level of an upper surface of the gate oxide layer.

19. The flash memory device of claim 14 wherein the wordline extends down past the level of an upper surface of the substrate.

20. A flash memory device comprising:

strings of adjacent transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate, the plurality of floating gates formed above a substrate;

wherein in the case of programming adjacent NAND strings, a channel of a first string adjacent a floating gate of a second string may be at a first potential for a number of programming pulses and changed to a second potential during subsequent programming pulses; and

means for controlling the floating gates and for isolating the floating gates from variations of adjacent potential fields during and between program pulses, the means for controlling the floating gates and for isolating the floating gates extending between the floating gates to or below the upper level of the substrate.

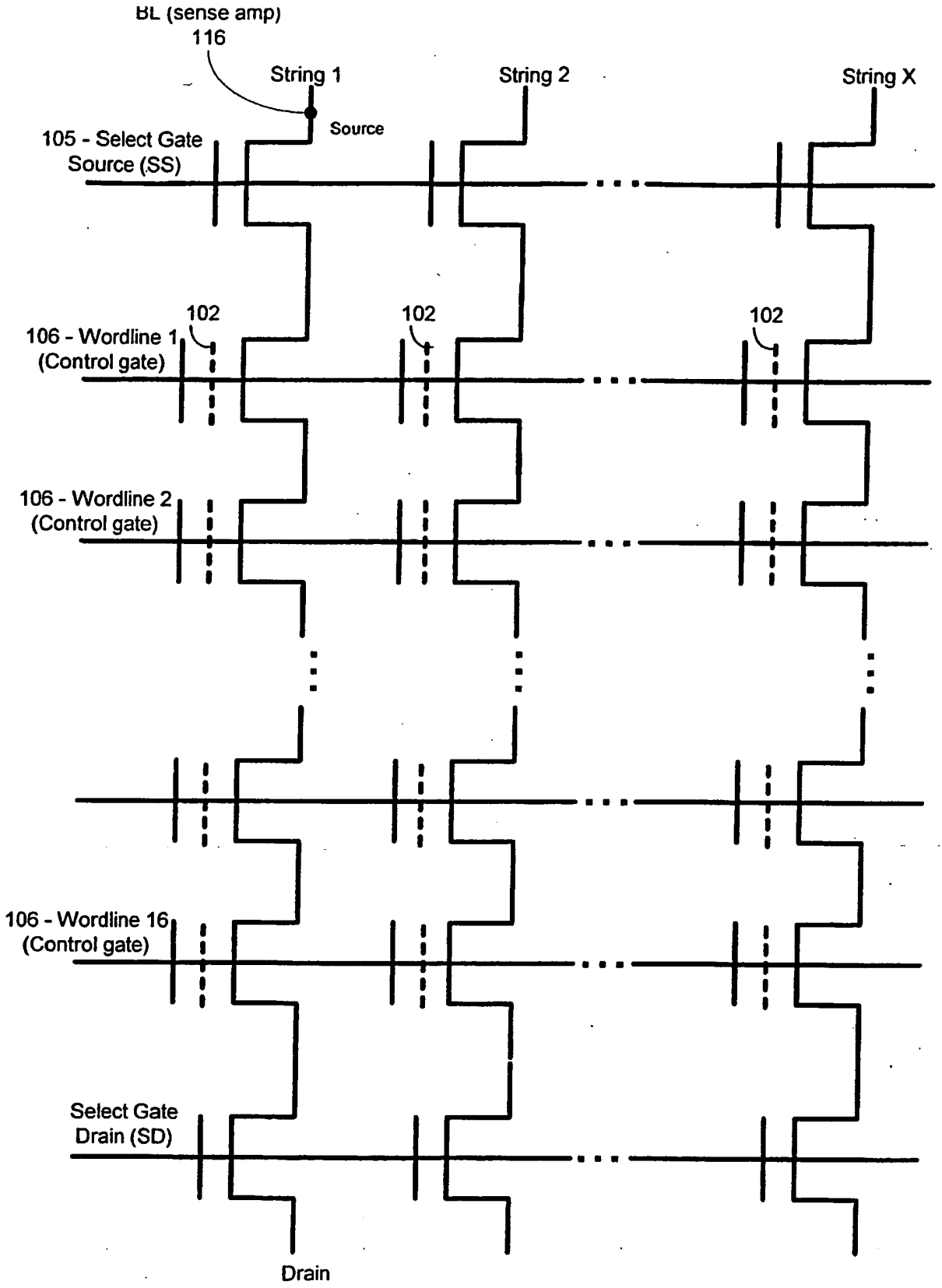


FIG. 1B

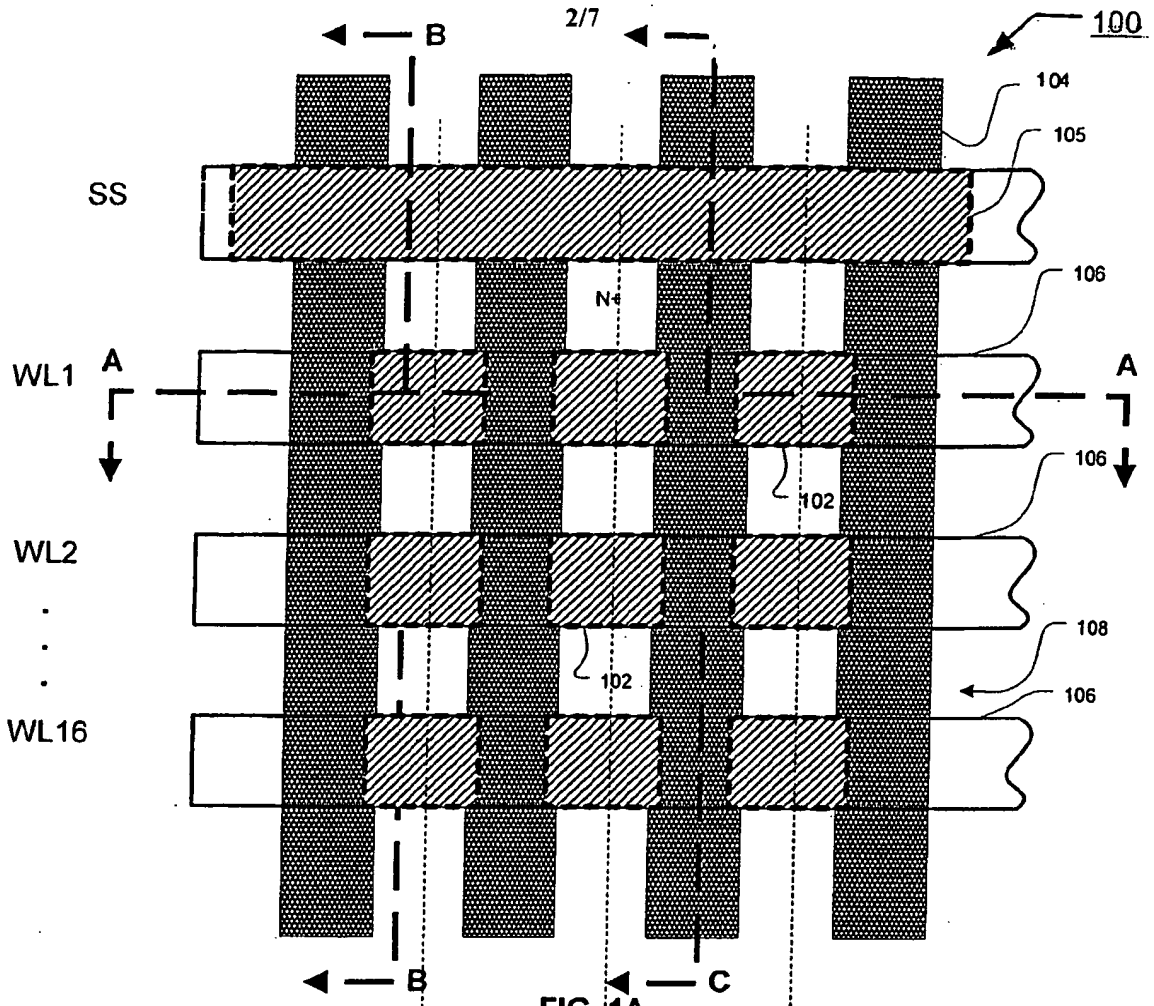


FIG. 1A

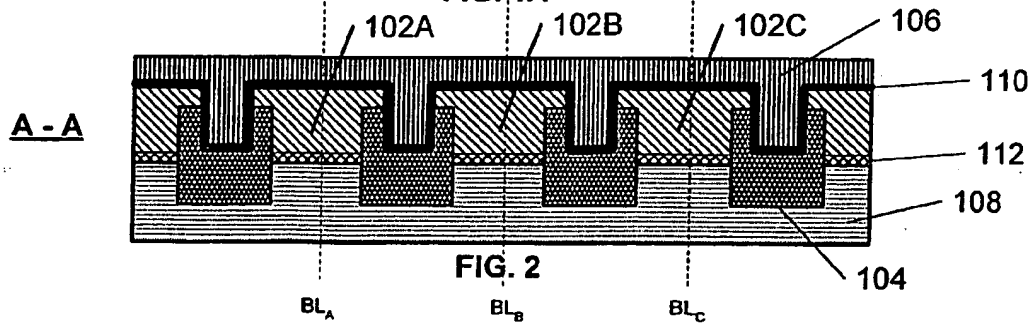


FIG. 2

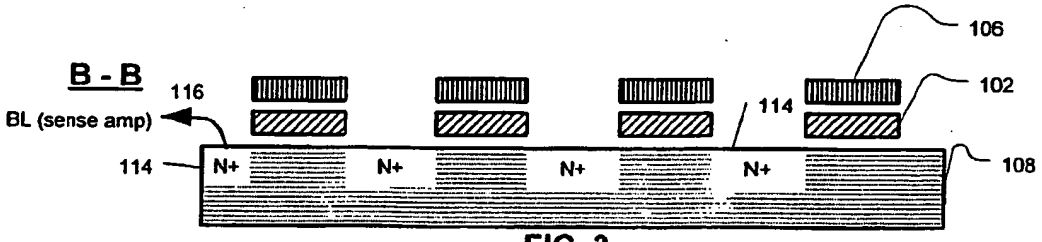


FIG. 3

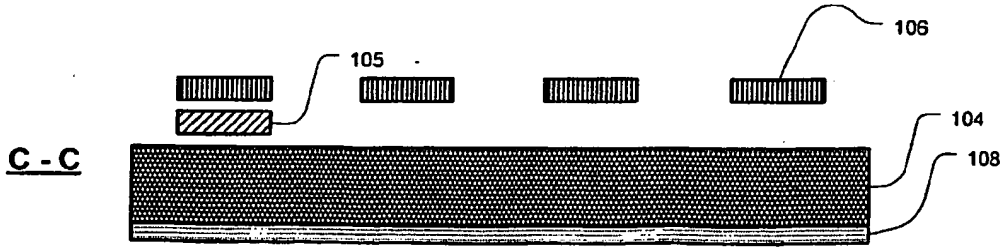


FIG. 4

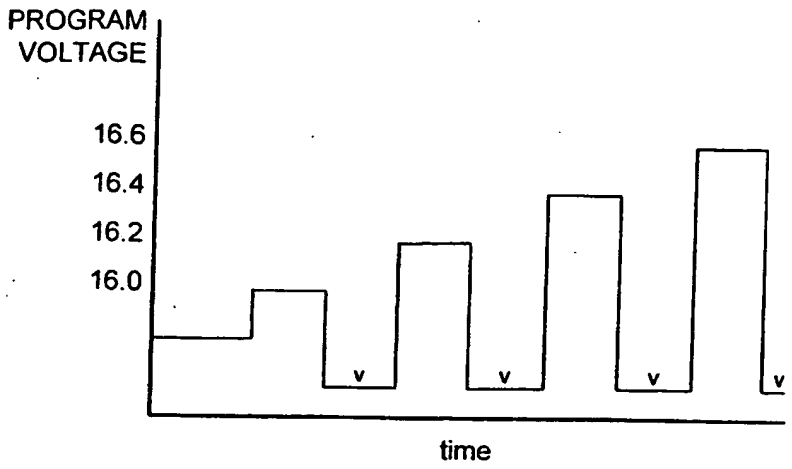


FIG. 5A

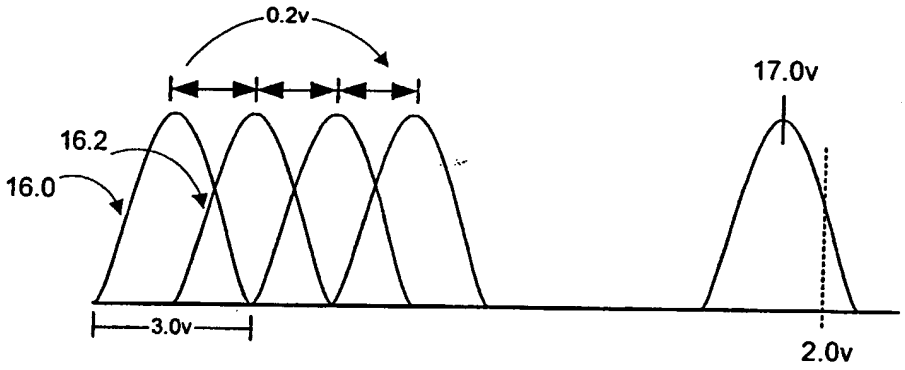


FIG. 5B

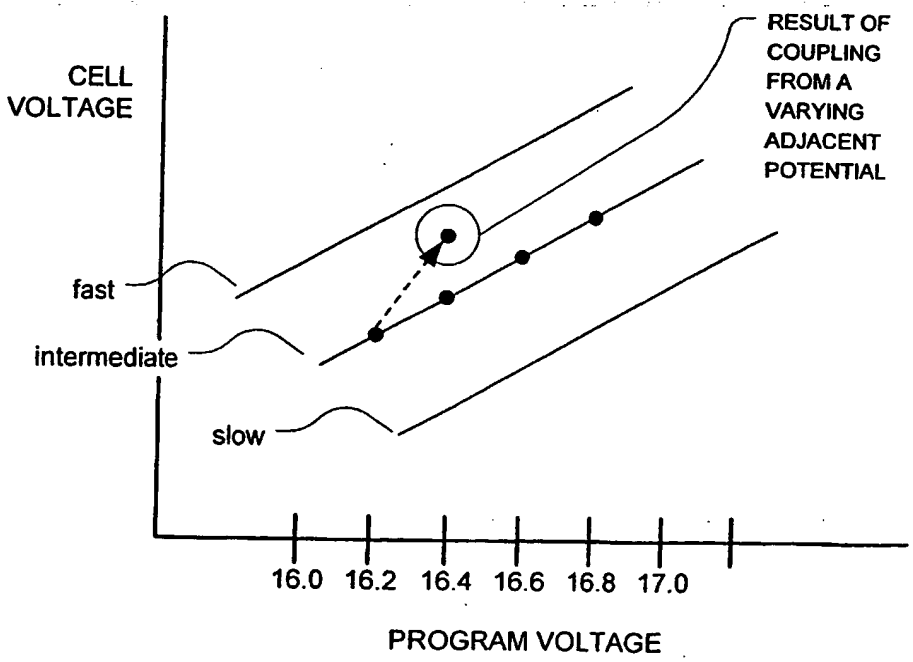


FIG. 5C

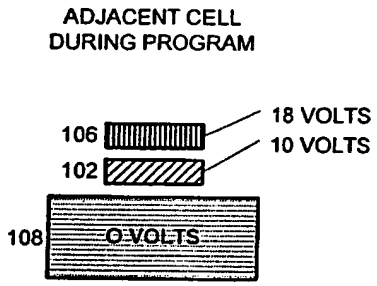


FIG.5D

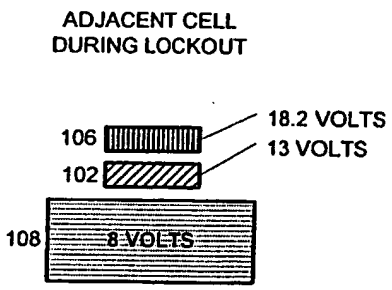


FIG.5E

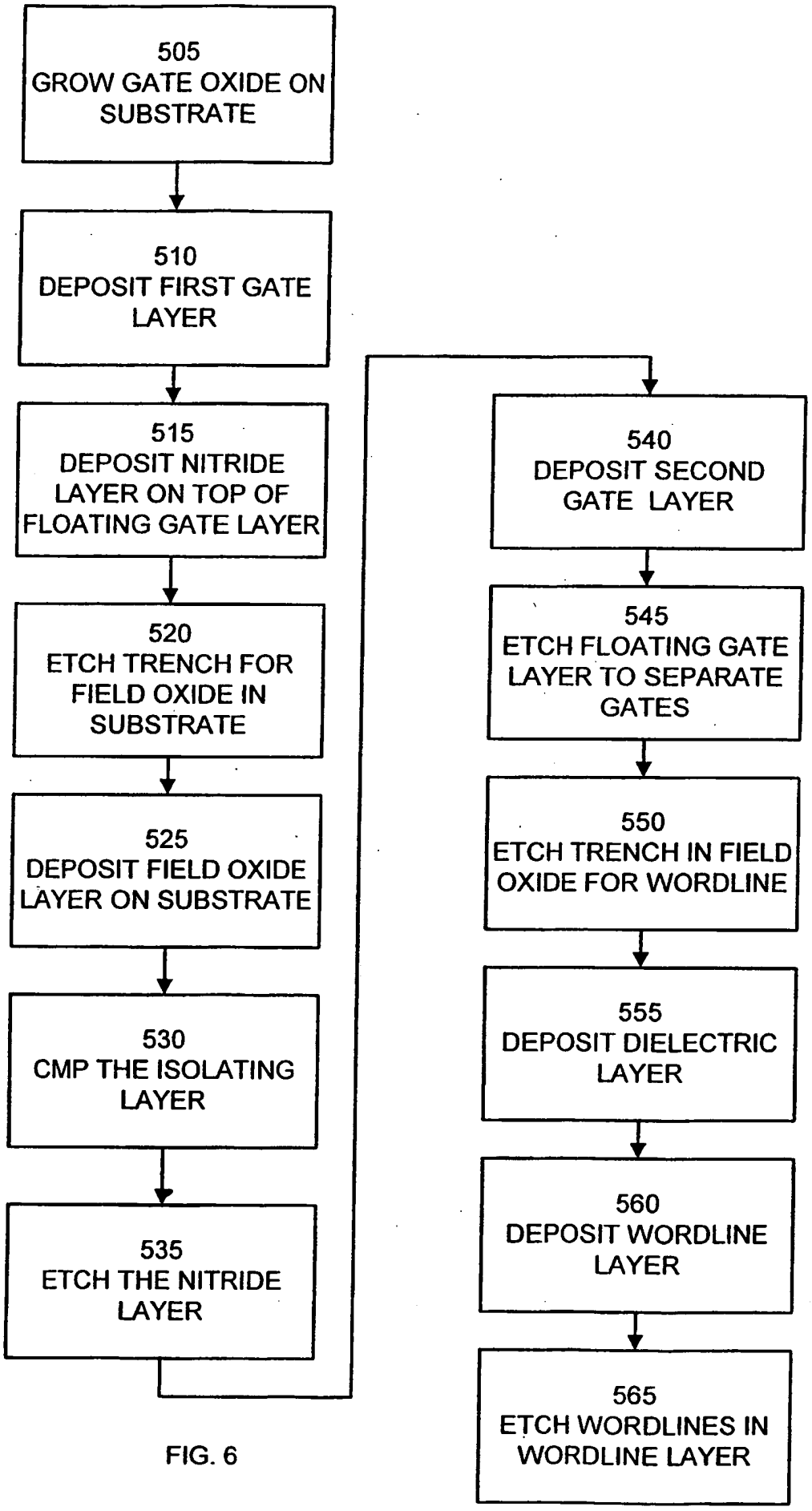


FIG. 6

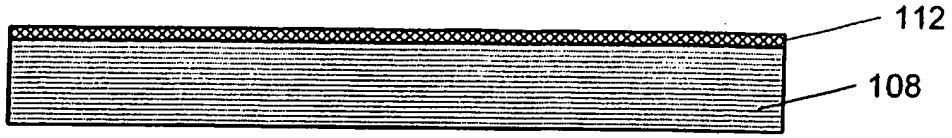


FIG. 7A

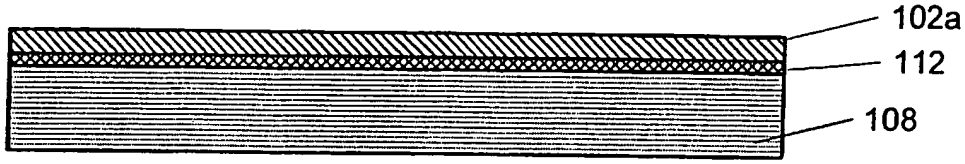


FIG. 7B

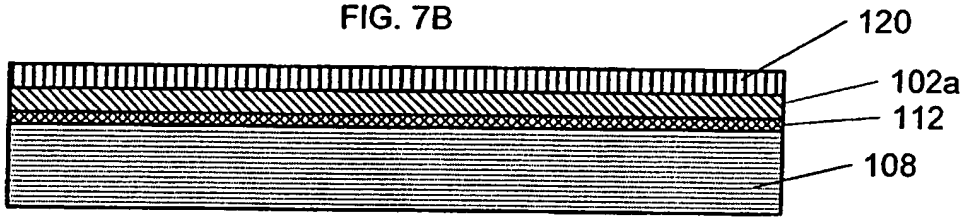


FIG. 7C

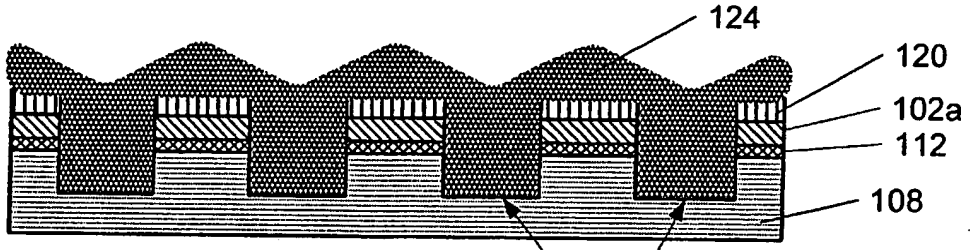


FIG. 7D

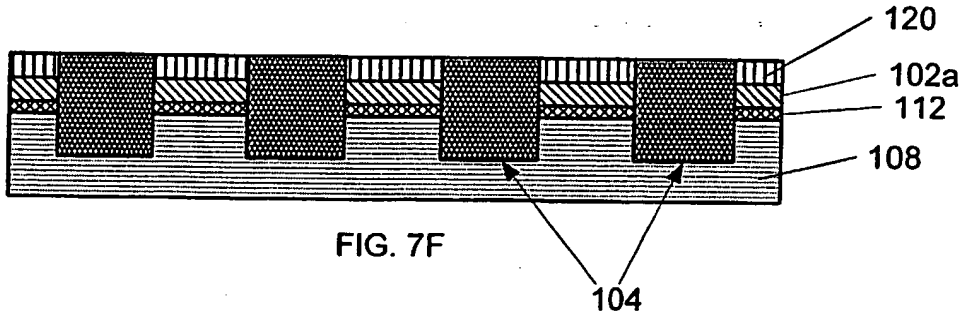


FIG. 7F

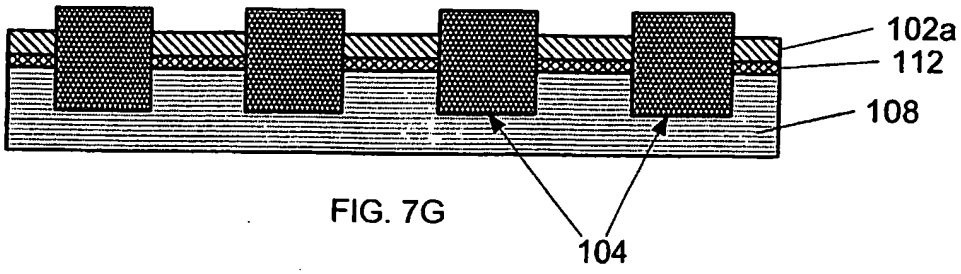


FIG. 7G

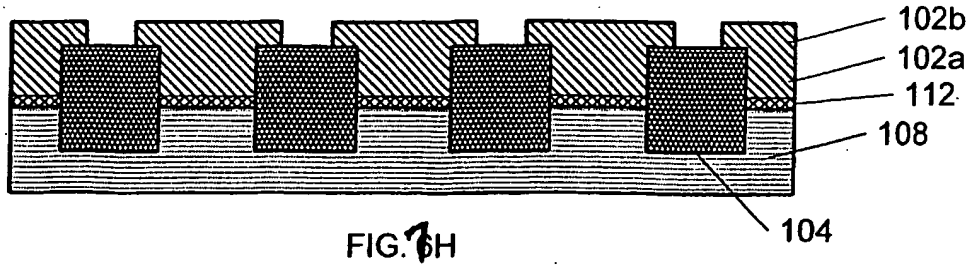


FIG. 7H

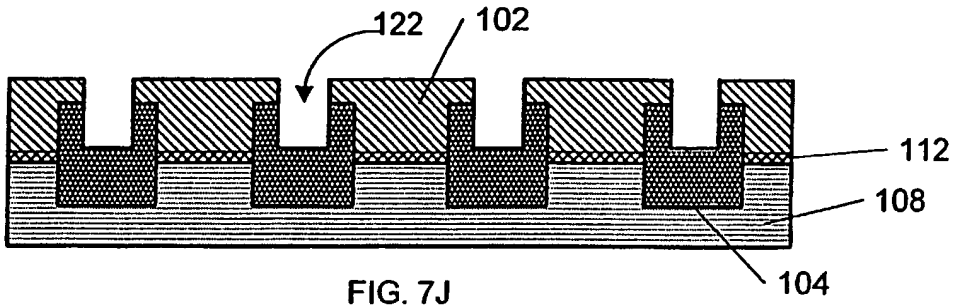


FIG. 7J

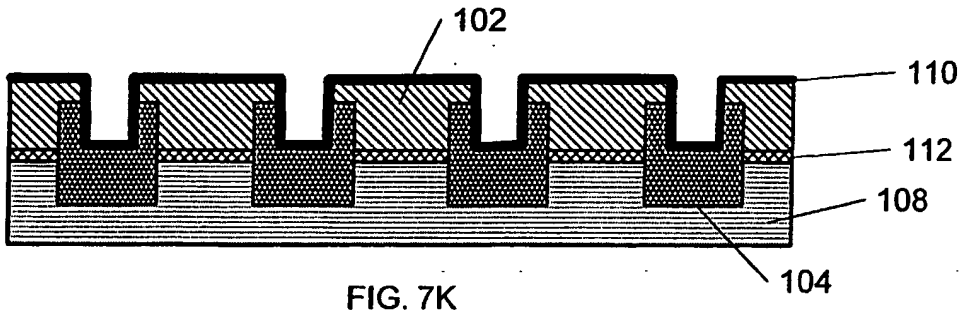


FIG. 7K

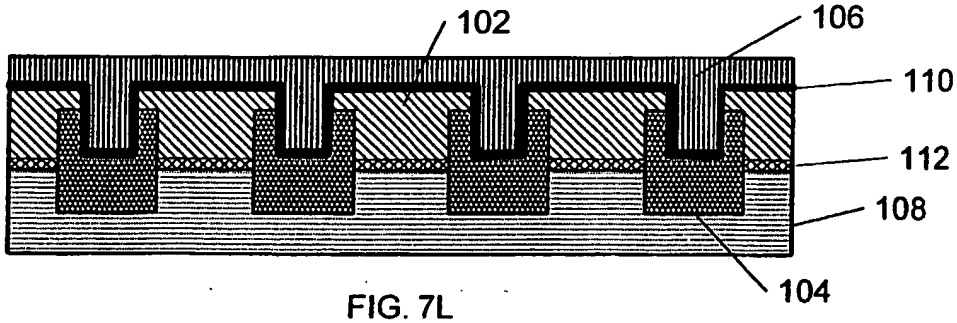


FIG. 7L

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/18183

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/115 H01L21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, COMPENDEX, INSPEC, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2001/001491 A1 (SAKUI KOJI) 24 May 2001 (2001-05-24) paragraph '0078! - paragraph '0137!; figures	1-20
A	US 5 640 032 A (TOMIOKA YUGO) 17 June 1997 (1997-06-17) column 5, line 35 -column 8, line 40; figures 1-7	1-20

[ ] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2003	03/11/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Blackley, W

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 03/18183

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001001491 A1	24-05-2001	JP 11145429 A	28-05-1999
		US 6214665 B1	10-04-2001
US 5640032 A	17-06-1997	JP 8130264 A	21-05-1996

Form PCT/ISA/210 (patent family annex) (July 1992)